## REMARKS

Claims 50 and 52 have been cancelled, and new claims 94 and 95 have been added. Thus, claims 1, 2, 4-33, 35-44, 46, 48, 54, 56, 92-95 are pending in this application. For at least the following reasons, it is respectfully submitted that this application is in condition for allowance.

Initially, it is noted that the total number of claims and the total number of independent claims are not changed by this amendment.

Before responding to this rejection, the amendment of claims is briefly explained. New claim 94 corresponds to the canceled claim 53, and new claim 95 corresponds to the canceled claim 55. In the Paper submitted on May 31, 2006, while Applicant intended to cancel claims 50 and 52, claims 53 and 55 are accidentally cancelled. Thus, in this amendment, the cancelled claims 53 and 55 are reinstated as claims 94 and 95, respectively, and claim 50 and 52 are canceled.

In the Action, Claims 1, 2, 6-28, 32-33, 37-42 and 45-56 are rejected under 35 U.S.C. 102 (b) as being anticipated by Miyajima. First, the invention defined in independent claims 1 and 32 relates to a sealing apparatus for sealing a semiconductor wafer having semiconductor elements on its surface by resin. The characteristic of the invention claimed in claims 1 and 32, and the differences between the invention defined in claims 1 and 32 and Miytajima are clearly

explained in the Paper submitted on September 28, 2005 on page 18, lines 5-13 (characteristic) and lines 14-20(differences). Namely, the characteristic of the invention claimed in claims 1 and 32 is,

(a) a lower mold having a first area where the semiconductor wafer is to be mounted, wherein the lower mold has an uneven surface, which is formed within a second area, which is in the first area, and wherein the uneven surface is not formed in the periphery of the first area.

As described in the specification of the present invention on page 10 lines 8-15, according to the structure described above, if the uneven surface exists under the periphery of the semiconductor wafer 201, large force may be focused on the periphery of the semiconductor wafer 201. As a result, the force in the range between a few tons and a few decades of tons is applied to the sealing device 100.

As to the differences from Miyajima, Miyajima does not disclose this characteristic at all. The device disclosed in Miyajima includes a lower die 20 having an area enclosed by sucking holes 76a. The surface in the area is mat-finished to form fine projections. As shown in Fig. 17, it is clear that the area enclosed by the sucking holes 76a is much larger than an area where a semiconductor wafer is placed. Thus, the fine projections are arranged under the peripheral area of semiconductor wafer when the semiconductor wafer is sandwiched between the upper and lower dies. Applicant understands that Miyajima discloses the device having fine projections at the bottom of the cavity. However, the fine projections are formed on the entire surface of the cavity in order to position a release film accurately. Please refer the column [0059] of

Miyajima. In addition, in Fig. 16 of Miyajima, the entire surface of the circular contacting-by-pressing side 20c, which contacts by pressing the semi-conductor wafer 90 and it periphery that is the entire area encompassed by the air adsorption holes 96, are formed with fine projections, and it is also clear from Fig. 17 that the fine projections are formed on the entire surface of the area which is encompassed by the air adsorption holes 76a. Therefore, Miyajima is quite different from the invention at the point that the uneven surface is not formed in the periphery of the first area.

However, as described above, the examiner addressed nothing as to the differences described above in the Action dated August 28, 2006. According to the MPEP 707.07 (f), it is clearly mentioned that where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it.. Thus, this time, I would respectfully request the examiner to address the applicant's argument and answer the substance of it.

Therefore, since Miyajima does not disclose or suggest the claimed sealing apparatus having the characteristic (a) described above, claims 1 and 32 clearly are not anticipated by Miyajima, and is deemed to be clearly patentable over Miyajima, and the rejection of claims 1 and 32 accordingly should be withdrawn.

Further, claims 2, 6-28, 33 and 37-42 depend from claim 1 or claim 32 directly or indirectly. Since Applicants believes that claims 1 and 32 includes a patentable subject matter, the rejection of claims2, 6-28, 33 and 37-42 depended from claim 1 or claim 32 should be withdrawn.

As to Claim 45-56, by this amendment, the family of independent claim 45 was cancelled, and only the family of the independent claim 46 remains by adding new claims 94 and 95, and the characteristic of the invention claimed in claim 46 is,

(b) shock absorbers buffering stress to the semiconductor wafer, wherein a part of each shock absorber is exposed in the area, and wherein the shock absorbers are disposed symmetrically against the center of the area.

As described in the specification on page 11 lines 9-18, according to the structure described above, in addition to buffering stress applied to the semiconductor wafer, the shock absorbers serve to adapt to the varieties of the thickness of each of the semiconductor wafers because they are located in the area where the semiconductor wafer is to be mounted, and because the plurality of shock absorbers are disposed in a balanced manner. As a result, the resin having uniform thickness can be formed even if the semiconductor wafers having a different thickness are set in the sealing apparetus defined in claim 46.

However, Miyajima does not disclose this characteristic at all. As the examiner suggested, the shock absorbers 78 are disclosed in Figs. 13-15. However, none of the shock absorbers 78 is exposed in the area where the semiconductor wafer is to be mounted. It is clear from Fig. 14 that the shock absorbers 78 is disposed outside an area where the semiconductor wafer is to be mounted. Thus, it may be difficult for Miyajima's device to a adapt to the varieties of the thickness of each of the semiconductor wafers.

In addition, in Fig. 16 of Miyajima, although it seems that the shock absorber 78 is disposed in a location facing to a good-to-be-mold 16, it should be

noted that the good-to-be-mold 16 is not a semiconductor wafer. This is clear from Fig. 14 that it shows the example of the resin sealed semiconductor wafer. Further, a good-to-be-mold 16 is mounted on the upper mold, not on the lower mold so that Miyajima has no idea that each shock absorber is exposed in the area, and that the shock absorbers are disposed symmetrically against the center of the area.

Therefore, since Miyajima does not disclose or suggest the claimed sealing apparatus having the characteristic (b) described above, claim 46 clearly is not anticipated by Miyajima, and is deemed to be clearly patentable over Miyajima, and the rejection of claim 46 accordingly should be withdrawn.

Further, claims 48, 54, 56, 94 and 95 depend from claim 46 directly or indirectly. Since Applicants believes that claim 46 includes a patentable subject matter, the rejection of claims 48, 54 and 56 depended from claim 46 should be withdrawn, and new claims 94 and 95 should be allowed.

In the Action, claims 5 and 36 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Miyajima. However, claims 5 and 36 depends from claims 1 and 32, respectively. Applicants believes that claims 1 and 32 include a patentable subject matter, the rejection of claims 5 and 36 depended from claims 1 and 32 should be withdrawn.

In the Action, Claims 29-31 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Miyajima in view of Yamamoto. Claims 29-31 are dependent claims, each of which depends from Claim 1 indirectly. Thus, these claim includes

all limitation of Claim1. As described above, Miyamoto does not disclose the characteristic (a) described above.

As to Yamamoto, it simply discloses a mold device for resin sealing. However, Yamamoto does not disclose a characteristic (a) described above at all.

Further, when a rejection depends on a **combination** of prior art references, there must be some teaching, suggestion, or motivation to combine the references. See, *In re Geiger,* 815 F.2d 686, 688 (Fed.Cir.1987). Moreover, three possible source for motivation to combine references are; (1) nature of problem to be solved, (2) the teachings of the prior art, and (3) knowledge of person of ordinary skill in the art. See also *In re Rouffet,* 149 F.3d 1350, 1357(Fed.Cir.1987). Yamamoto discloses that a lead frame on which a semiconductor chips is mounted is sealed by resin, not that a semiconductor wafer is sealed. Thus, since the nature of the problem to be solved at least is not identical between Miyajima and Yamamoto, these references cannot be combined. Actually this argument had been made in Paper submitted on September 28, 2005, but the examiner did not address to this argument. I would respectfully request the examiner to address this issue if the examiner maintains the position as to the combination of Miyajima and Yamamoto.

Accordingly, neither Miyajima nor Yamamoto suggest or disclose the characteristic described above, claims 29-31 clearly are not obvious over Miyajima in view of Yamamoto, and is deemed to be clearly patentable over them, and the rejection of claims 29-31 accordingly should be withdrawn.

In the Action, Claims 4, 35, 92 and 93 are rejected under 35 U.S.C. 103 (a)

as being unpatentable over Miyajima in combination with Tago. The characteristic of the invention claimed in claims 4 and 35 includes that the uneven surface has a roughness in a range between 8μm and 12μm. According to this structural characteristic, it is possible to avoid making any damage to a semiconductor wafer, and to avoid adhering a semiconductor wafer to the mold.

However, First of all, Miyajima does not disclose or suggest any size of the fine projection. As examiner well pointed out, Miyajima fails to teach forming a wafer pr substrate directly on the surface of mold or lower mold. In other words, a release film exists between the cavity and a semiconductor wafer. Thus, fine projections do not touch the semiconductor wafer directly. From this structural reason, Miyajima has no idea to avoid making a scratch on the semicondcutror wafer by considering the size of the fine projection. On the other hand, the semiconductor wafer directly placed on the rough surface in the present invention, and when the uneven surface is set in a roughness in a range between 8μm and 12μm, it would be possible to avoid making scratches on the semiconductor surface.

As to the combination with Tago, as well as Yamamoto, Tago discloses that a lead frame on which a semiconductor chips is mounted is sealed by resin, not that a semiconductor wafer is sealed. Thus, as explained above as to the issue of the combination matter, since the nature of the problem to be solved at least is not identical between Miyajima and Tago, these references cannot be combined.

Accordingly, neither Miyajima nor Tago suggest or disclose that the uneven surface has a roughness in a range between 8μm and 12μm, claims 4 and 35 clearly are not obvious over Miyajima and Yamamoto, and is deemed to be clearly

patentable over them. Claims 92 and 93 depend from claims 4 and 35, respectively so that claims 92 and 93 should also be patentable.

Claims 43 and 44 are allowed.

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any fee be needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Respectfully submitted,

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